Integrated circuit clock mesh synthesis with clock gating

**Technology Summary:** A clock mesh network has been the preferred clock network structure for high-end microprocessor design because of its tolerance to variations. The variation tolerance is achieved by placing the redundant mesh grid wires near the sink registers, but at the cost of power dissipation. To overcome the limitations of existing clock mesh networks, a team of Drexel researchers has developed a clock mesh network synthesis method which enables clock gating on the local sub-trees of the clock mesh network in order to reduce the clock power dissipation. Clock gating is performed with a register clustering strategy that considers both i) the similarity of switching activities between registers in a local area and ii) the timing slack on every local data path of the design area. The method encapsulates the efficient implementation of the gated local trees and activity driven register clustering with timing slack awareness for clock mesh synthesis. With gated local tree and activity driven register clustering, the switching capacitance on the mesh network can be reduced by 22% with limited skew degradation. The method has modes of low power and high performance to serve different design purposes.

**Applications:**
- High End Microprocessor Designs
  - Clock Network Structures

**Advantages:**
- **Lower Power Consumption** - power consumption of the clock mesh network is reduced compared to previous clock mesh design methods due to the combination of clock gating, steiner tree connection and the register clustering.
- **Timing Closure** - the non-negative timing slack of the circuit is preserved after the incremental register placement. The slack decrease tolerance is designer-specified.
- **Register Placement Optimization** - the incremental register placement is performed in local areas only, which preserves the placement optimization for timing and routing.

**IP Status:** Patented - US Patent No. 8,704,577

**Commercialization Opportunities:** Drexel is currently seeking commercial partners to license and/or sponsor research to further develop this technology.

**Inventors:** Baris Taskin, Jianchao Lu
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Contact Information

For Technical Information: Baris Taskin, Ph.D.
Associate Professor
Department of Electrical and Computer Engineering
Drexel University
3141 Chestnut Street
Philadelphia, PA 19104-2875
Phone: (215) 895-5972
E-mail: taskin@coe.drexel.edu
Web: http://vlsi.ece.drexel.edu

For Intellectual Property and Licensing Information: Paul Dougherty
Licensing Manager
Office of Technology Commercialization
The Left Bank
3180 Chestnut Street, Suite 104
Philadelphia, PA 19104
Phone: 1-215-571-4290
Email: pdougherty@drexel.edu